shaping tomorrow with you

Implementation and Application of Gate Voltage in NEGF Calculations

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My 2nd Visit to South Korea This Month

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Oct. 30 – Nov. 3
7th A3 Symposium on Emerging Materials
Buyeo, 2.5 h

Nov. 24 – 25
2nd OpenMX Developer's Meeting
Daejeon, 3 h

Outline

- Introduction
  - Motivation and Significance for the Implementation of a Gate Function in NEGF Calculations
- Implementation of a Gate Function
  - Symmetric Zigzag Graphene Nanoribbon Spin Filter
- Application to All Two-Dimensional (2D) Tunneling Field Effect Transistors (TFETs)
  - P-doped GeSe/MoS_2/VS_2 TFETs
- Summary

Introduction

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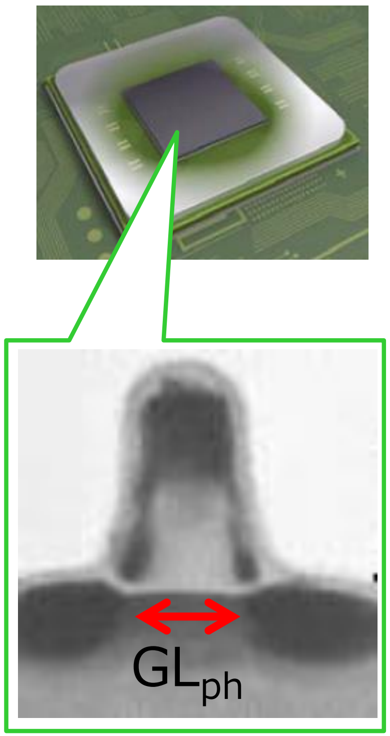
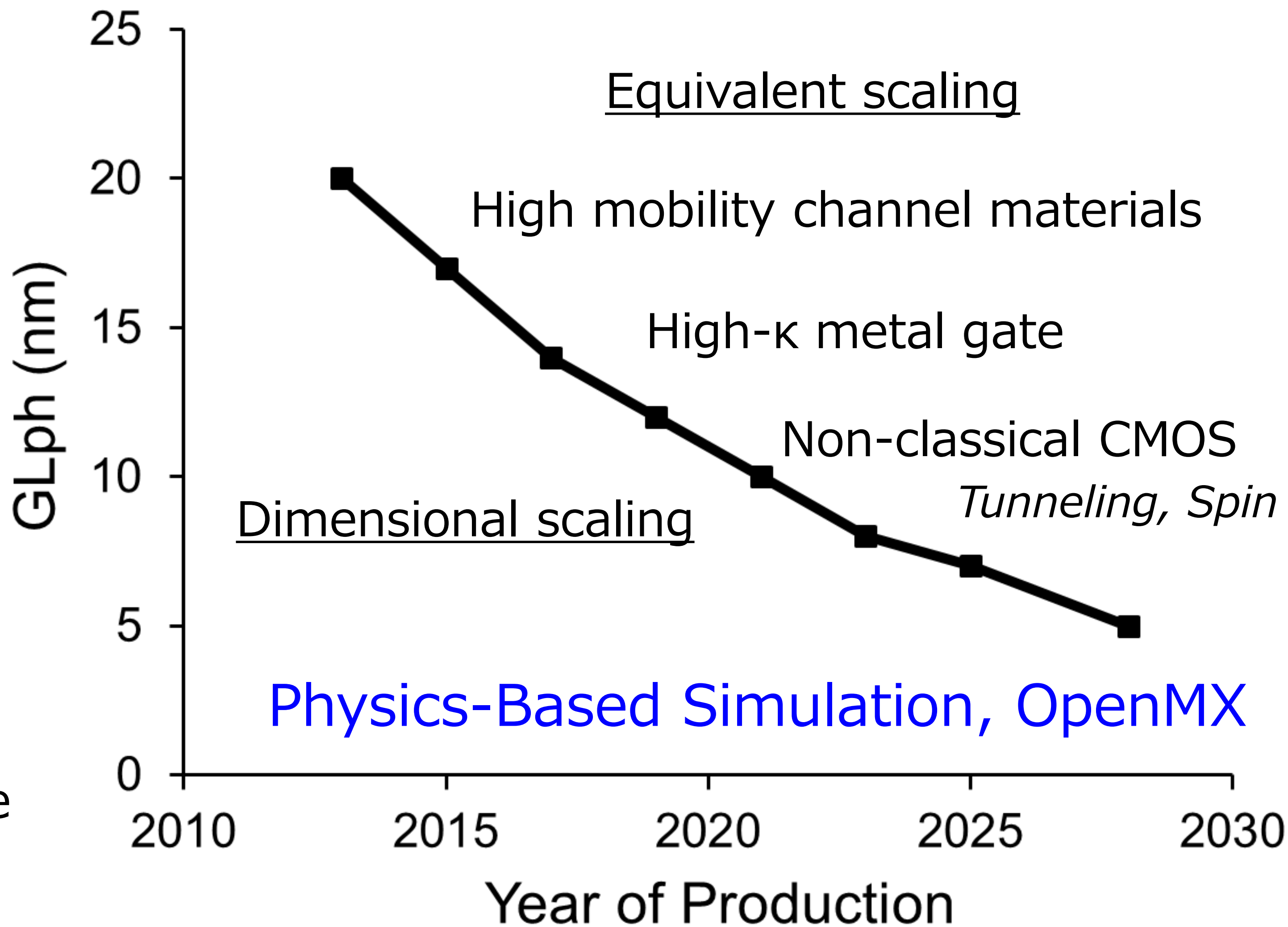
MPU High-Performance Physical Gate Length

MPU

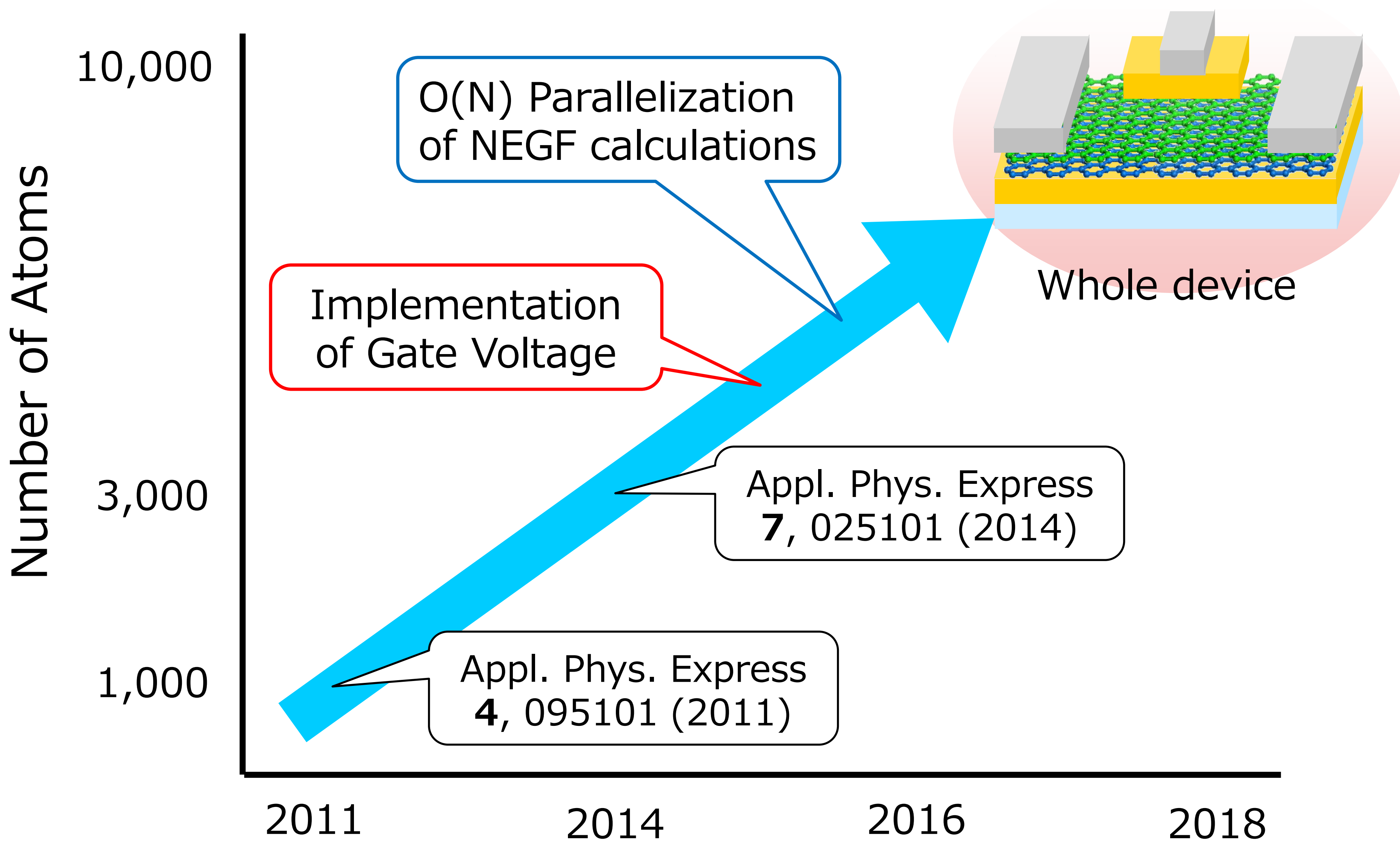
Micro processor unit



MOS (metal oxide semiconductor) transistor



Toward Whole-Device Simulations



Implementation of a Gate Function

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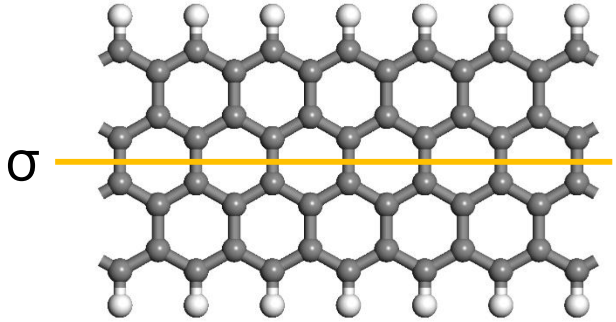
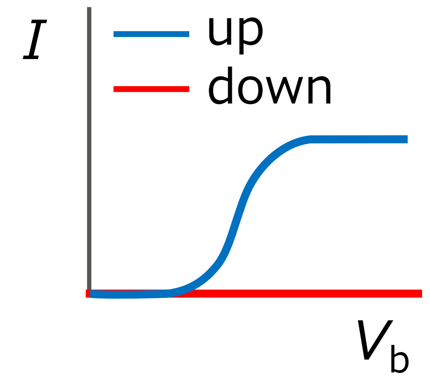
Symmetric Zigzag Graphene Nanoribbon Spin Filter[1]

[1]T. Ozaki et al., PRB **81**, 075422 (2010).



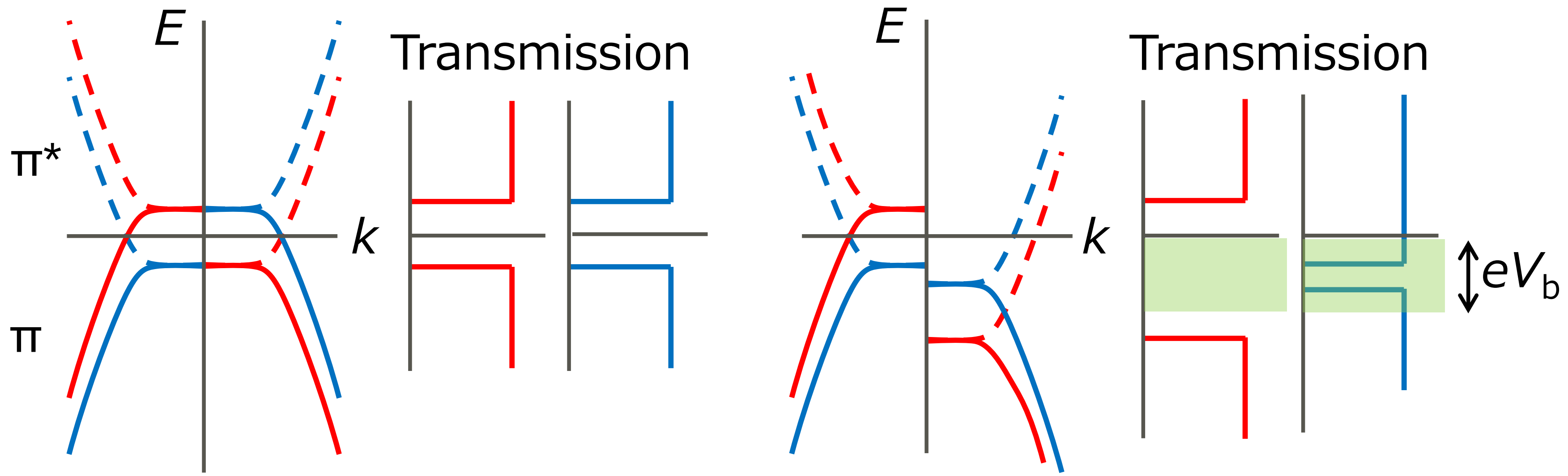
π: symmetric

π*: antisymmetric



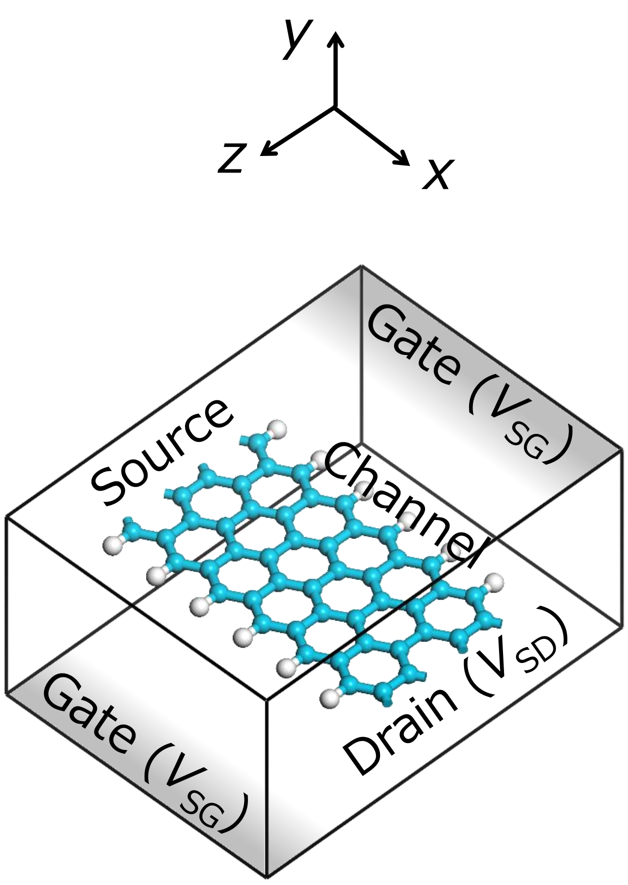
Antiferromagnetic junction

$V_b = 0$ $\qquad$ $V_b > 0$



Model for tests of the implementation

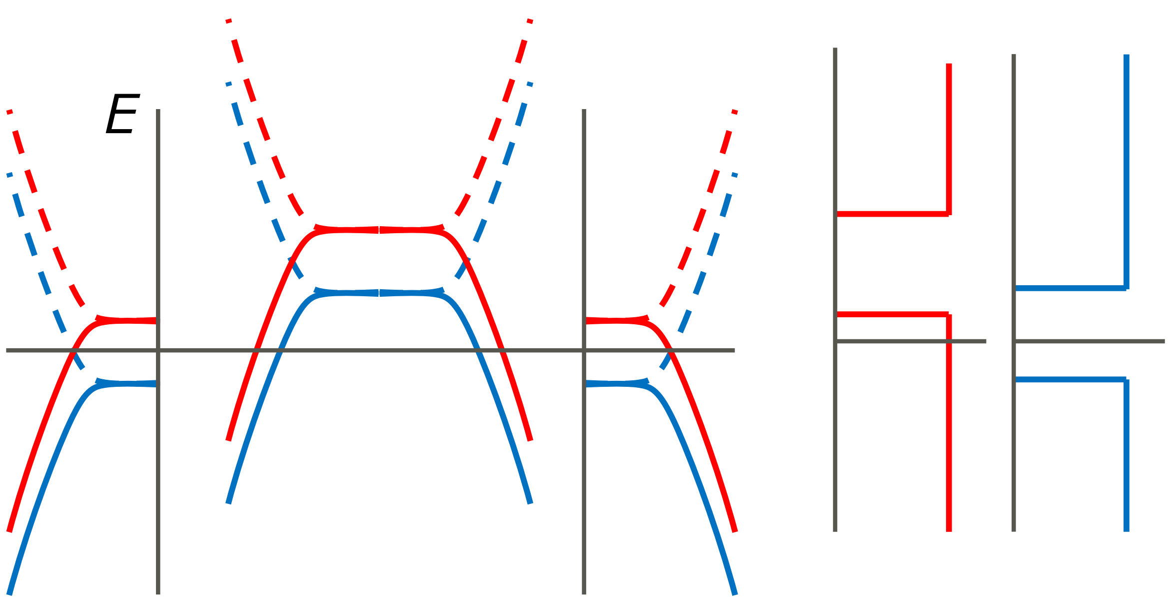
Symmetric Zigzag Graphene Nanoribbon



Double gate structure

Ferromagnetic junction

$V_{SG} < 0$



3D Poisson equation

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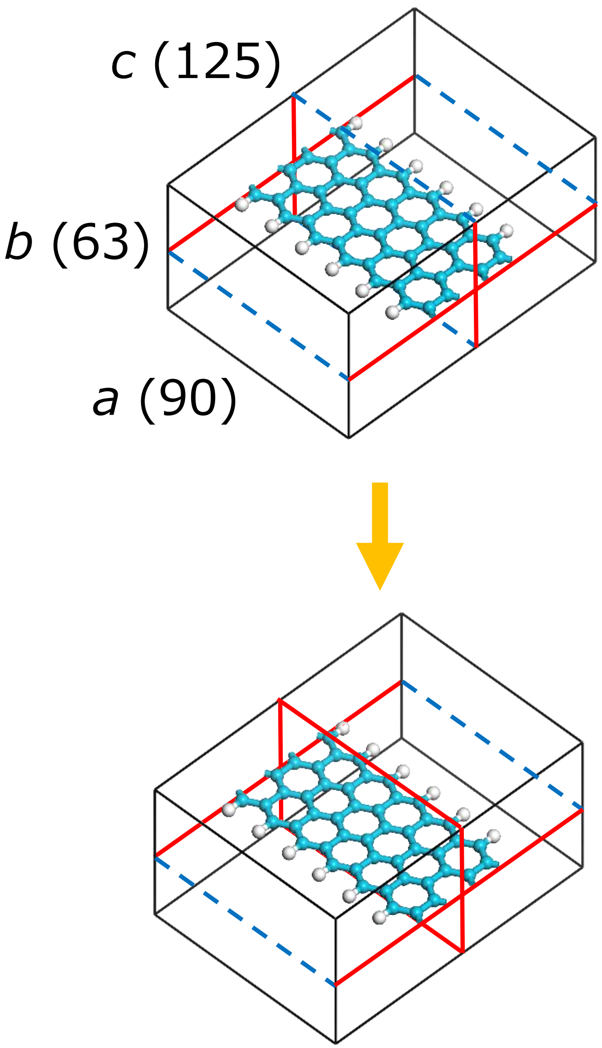
Boundary condition (BC)

Open BC (red solid line)   Periodic BC (blue dashed line)



$$\left(\frac{\partial}{\partial x^2} - k_y^2 - k_z^2\right)\varphi(x, k_y, k_z) = -\frac{4\pi}{\varepsilon_0}\rho(x, k_y, k_z)$$

Parallelization in bc plane (63x125)

$$\left(\frac{\partial}{\partial x^2} + \frac{\partial}{\partial y^2} - k_z^2\right)\varphi(x, y, k_z) = -\frac{4\pi}{\varepsilon_0}\rho(x, y, k_z)$$

Parallelization in only c line (125)

Programing

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Modification of only 10 Files

tran_variables.h
openmx_common.h
lapack_prototypes.h
tran_prototypes.h
Allocate_Arrays.c
Free_Arrays.c
init_alloc_first.c
truncation.c: Preparation for transforming from AB to C partition
TRAN_Input_std.c
TRAN_Poisson.c — TRAN_Poisson_FDG

- FFT for the boundary conditions
- Transformation from AB to C partition
- 2D real space Poisson equation
- Transformation from C to AB partition
- FFT to real space

Hartree Potential (eV)

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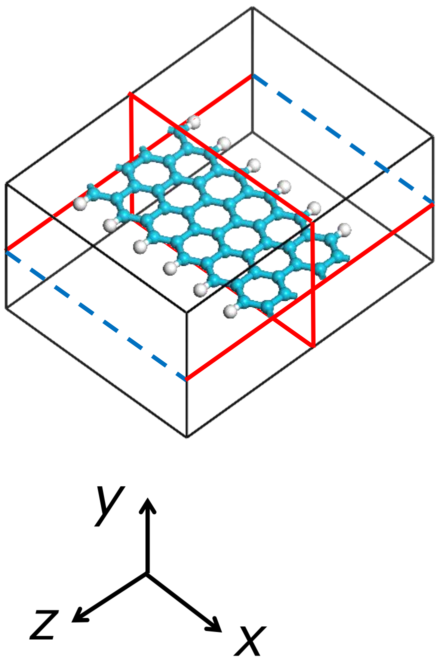
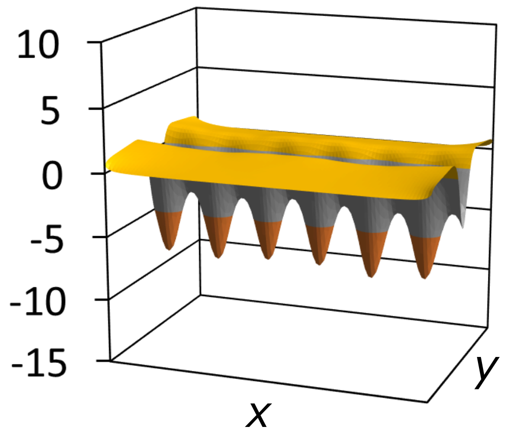
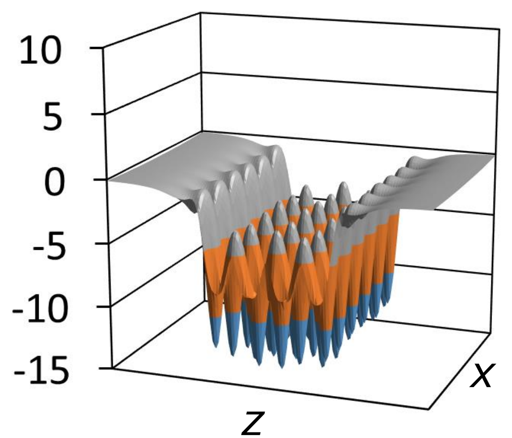
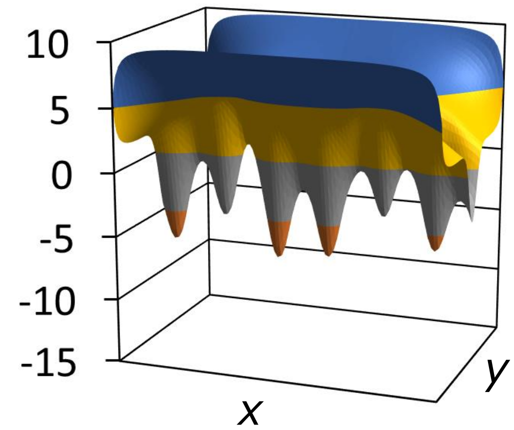


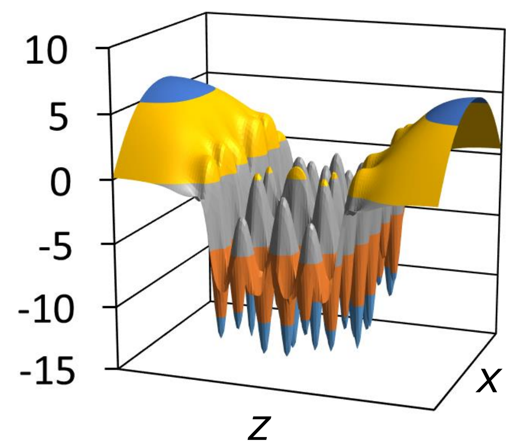
V_{SD} = 0 V, V_{SG} = 0 V





V_{SD} = 0.3 V, V_{SG} = −10 V

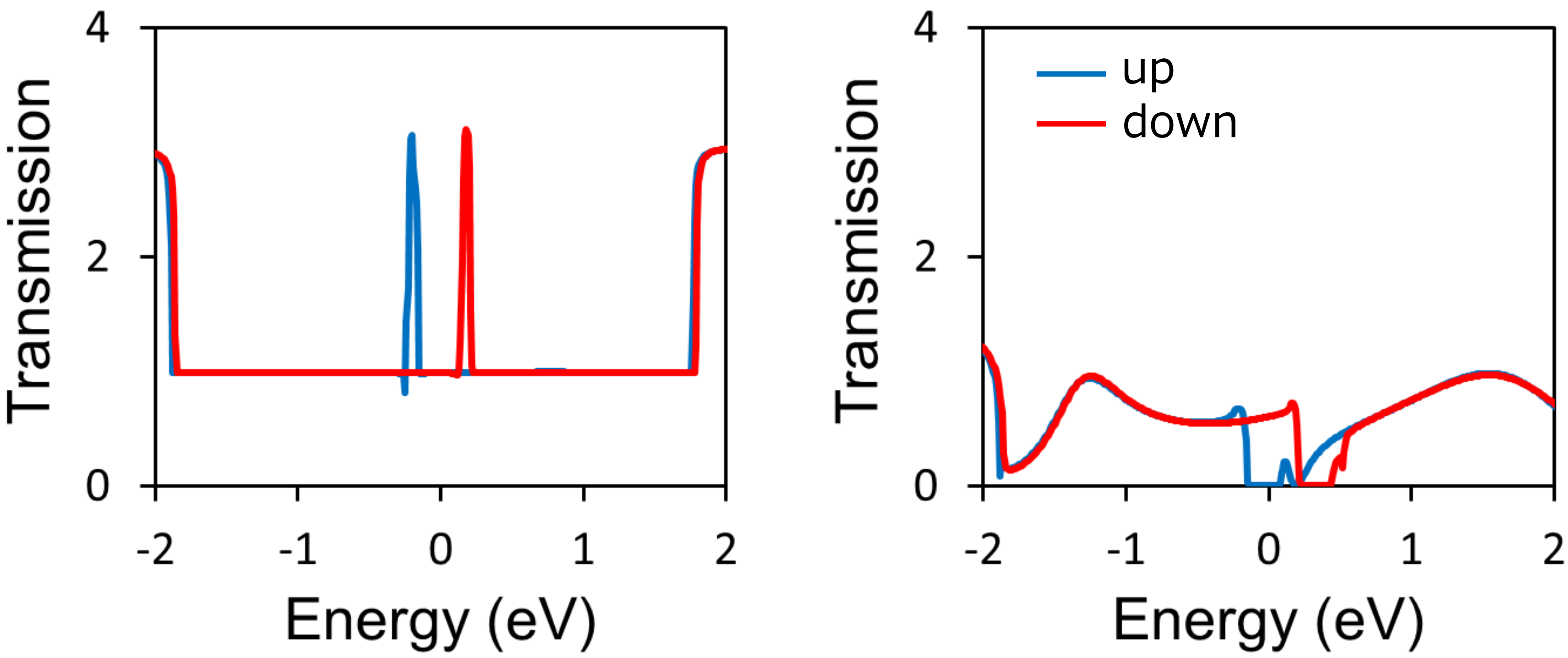


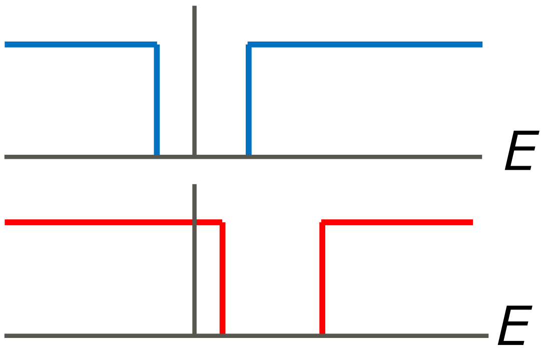


Transmission

V_{SD} = 0 V, V_{SG} = 0 V

V_{SD} = 0.3 V, V_{SG} = −10 V





This provides another possible spin filter.

All 2D Material Tunneling FETs

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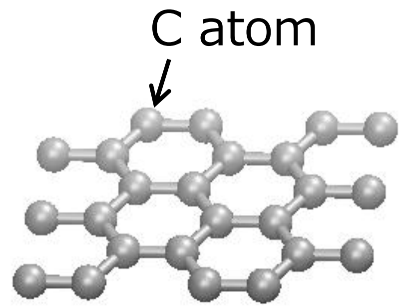
Graphene — Discovery (2004)



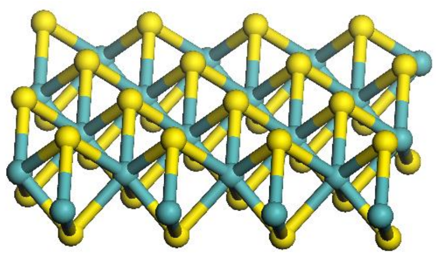
graphene

hBN

B	C	N

Transition metal dichalcogenide (TMDC)

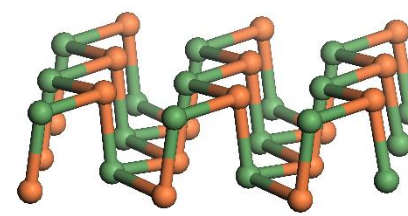
Ti	V	Cr		S
Zr	Nb	Mo		Se
Hf	Ta	W		Te


MoS_2

Phosphorene

Group-IV monochalcogenide

	P	S
Ge		Se
Sn		Te


GeSe

$GeSe/MoS_2/VS_2$ Tuneling FETs (TFETs)

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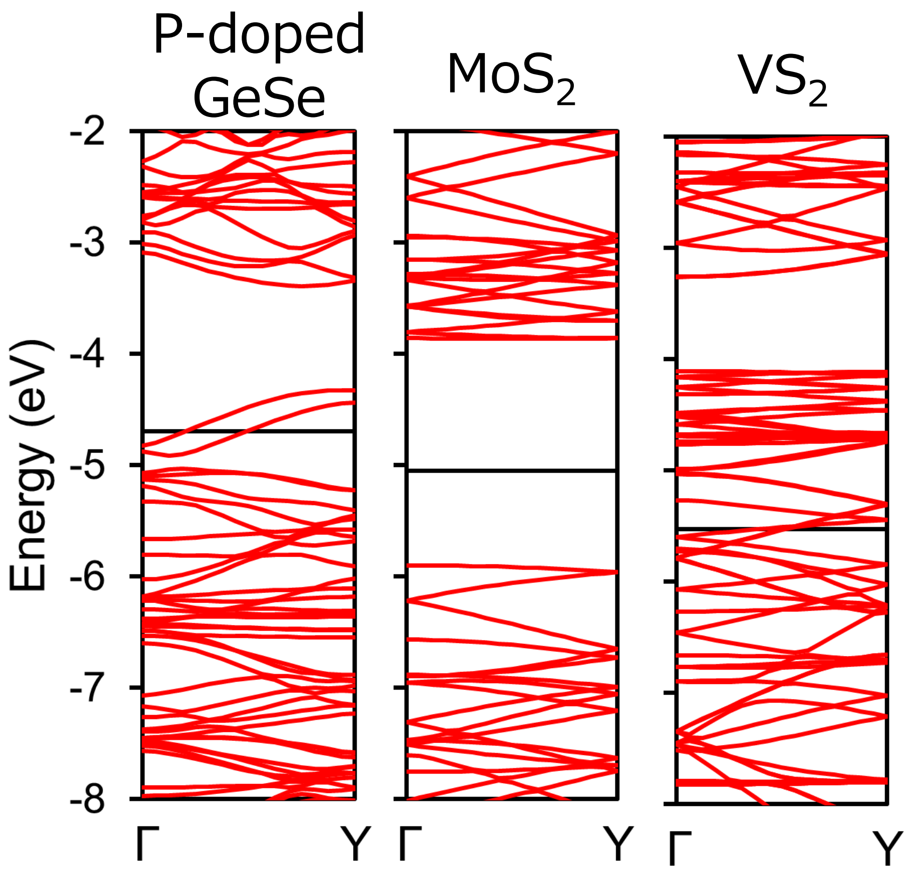
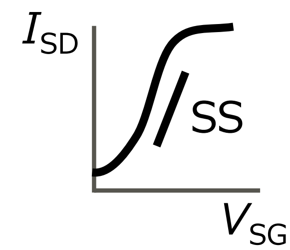
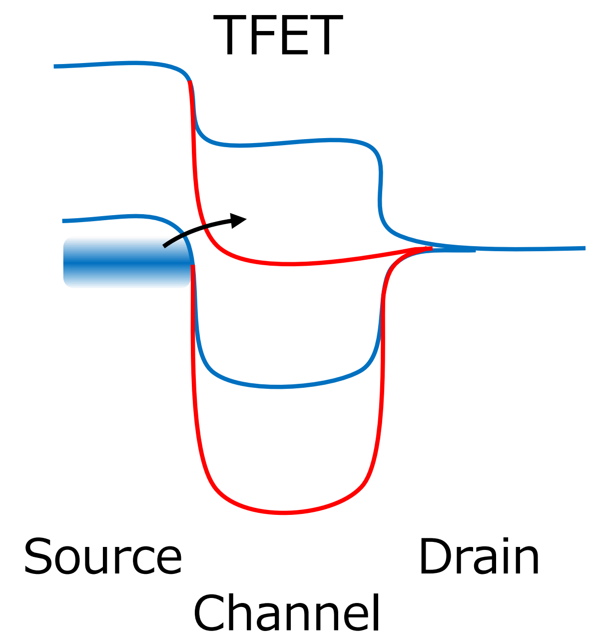


The subthreshold swing (SS) in conventional FETs is limited to 60 mV/dec.





The lattices of these materials are matched with a relatively small unit cell.

Computational Details

- DFT code: OpenMX
- Exchange-correlation potential:

  GGA-PBE with van der Waals correction
- Norm-conserving pseudopotential:

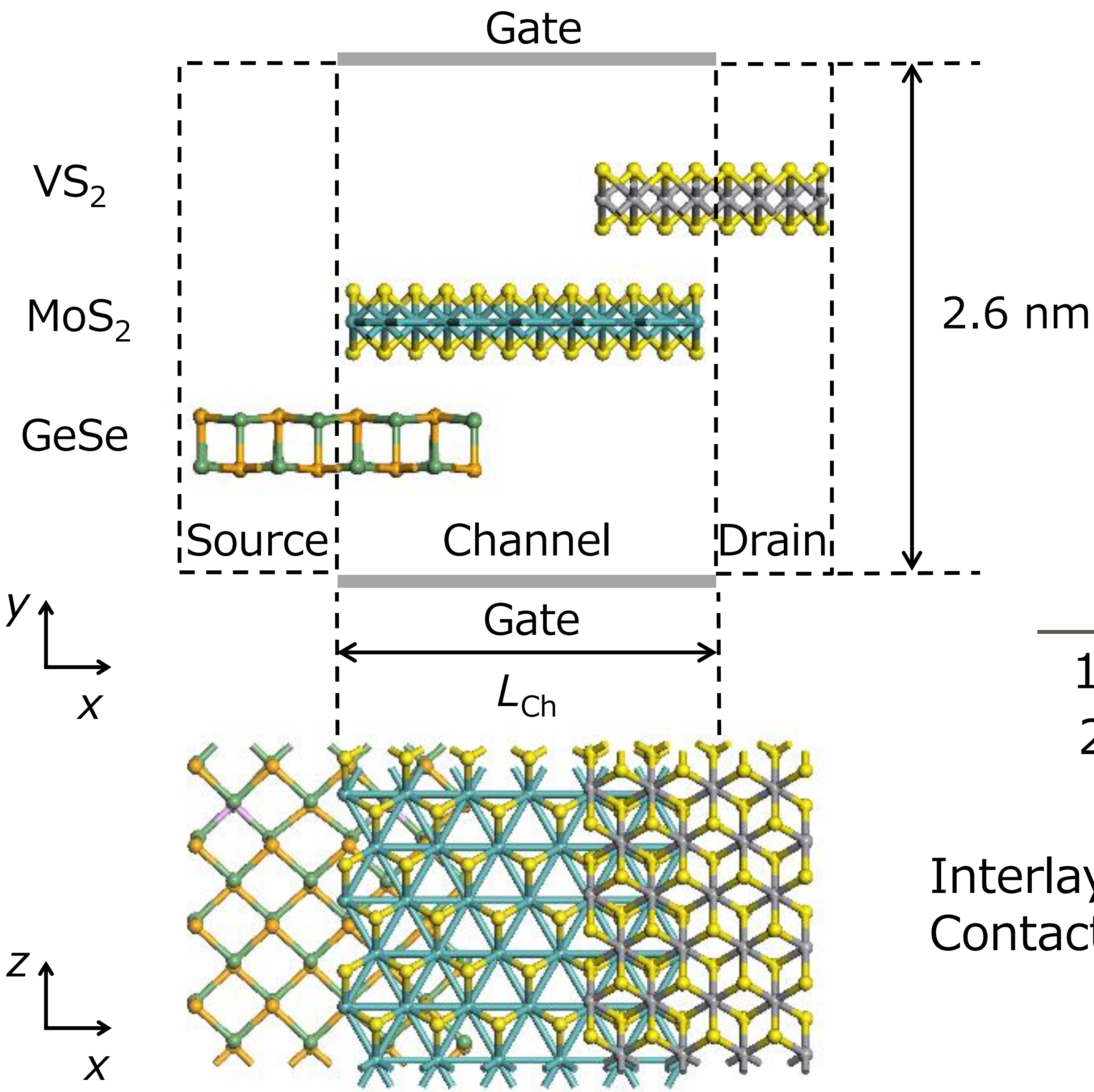
  Troullier-Martins
- Pseudo atomic orbitals (PAOs)

  Geometry optimization:

  Ge7.0-s3p3d3f2, Se7.0-s3p3d2f1, P7.0-s3p3d2f1, Mo7.0-s3p2d2f1, S7.0-s3p3d2f1, V6.0-s3p3d2

  Transport: s2p2d1
- Temperature: T = 300 K

Atomic Structure

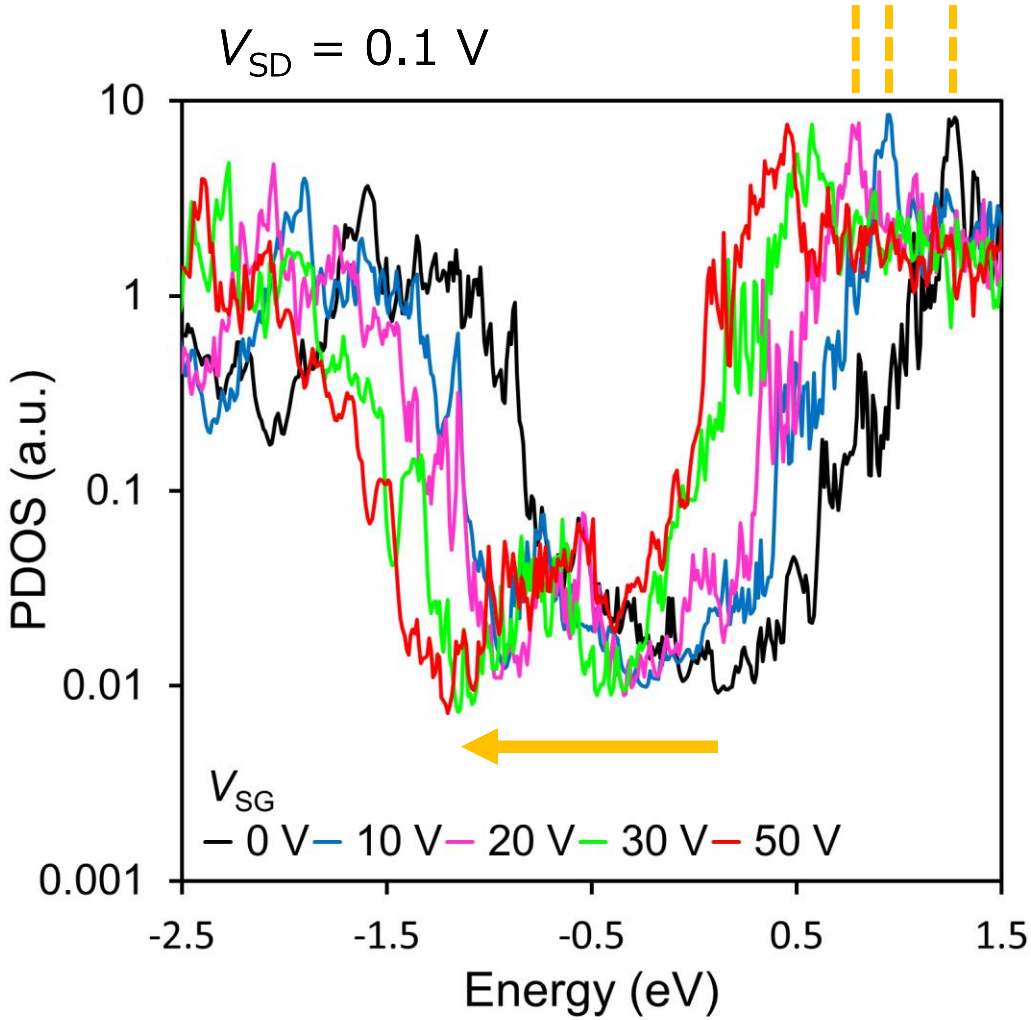


L_{Ch}	Number of atoms
1.9 nm	244
2.6 nm	280

Interlayer distance: 0.323 nm
Contact length: 0.6 nm

Gate Control

Partial density of states (PDOS) of Mo atom in the center of the channel (L_{Ch}=1.9 nm)



Device Properties

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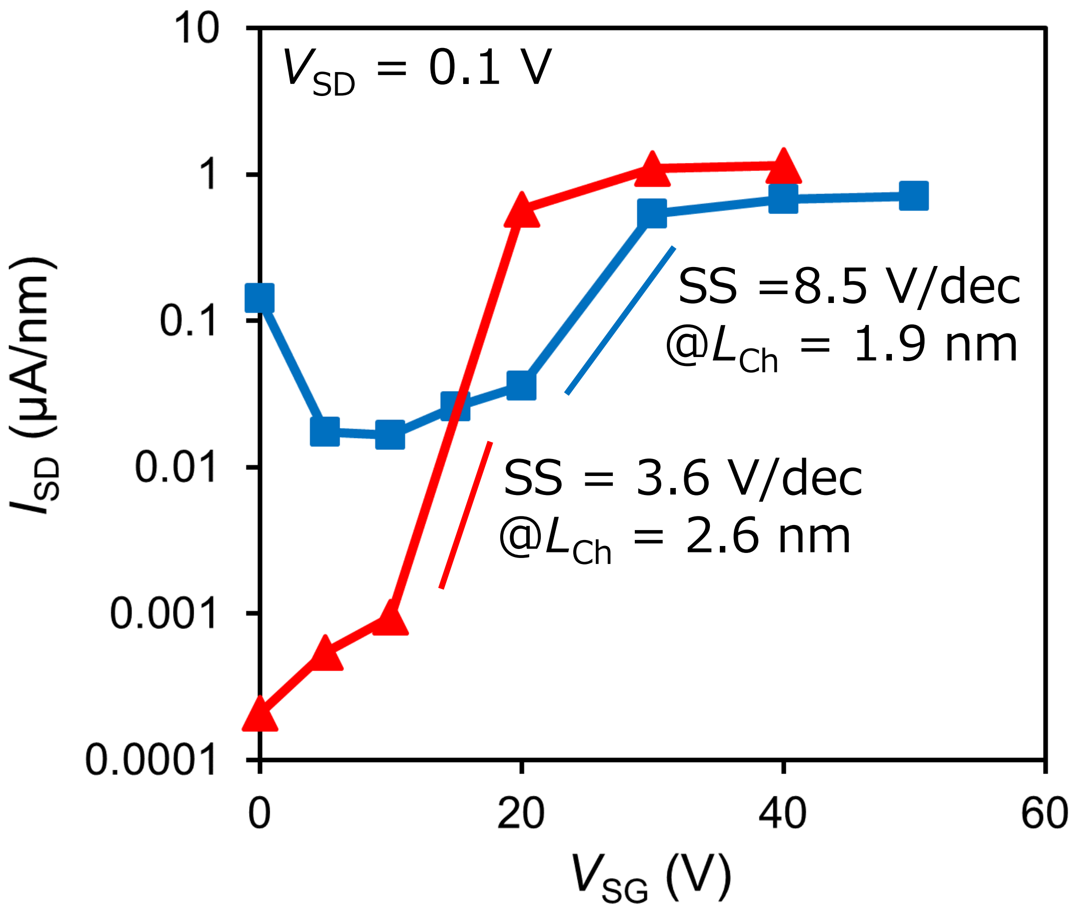

L_{Ch}	I_{on}/I_{off}
1.9 nm	> 10
2.6 nm	> 10^3

The subthreshold swing (SS) would be further improved by using a high-κ material as a gate dielectric that is a vacuum in the present model.

Computational Cost

Computer: Fujitsu PRIMERGY CX400

Information Technology Center,
Nagoya University
568 nodes
28 cores (128 GB)/node

L_{Ch} (nm)	Number of atoms	Number of mpi	Number of threads	Time (day)
1.9	244	105	7	1.5
2.6	280	105	7	2.7

We need further parallelization of Poisson equation calculation.

Summary

- We implemented a gate function in OpenMX (DFT-based NEGF code), by applying open boundary conditions to the 3D Poisson equation.
- We designed GeSe/MoS_2/VS_2 TFETs and examined the device properties using the developed code.
  - $I_{on}/I_{off} > 10$, SS = 8.5 V/dec @ L_{Ch} = 1.9 nm
  - $I_{on}/I_{off} > 10^3$, SS = 3.6 V/dec @ L_{Ch} = 2.6 nm
- This could be a powerful tool for exploring novel nanoelectronic and spintronic devices.

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